REMARKS

Claim Rejection Under 35 USC 112

Claims 4, 13, 16, 20 and 24 are rejected as failing to comply with the written description requirement of 35 USC 112 because the claimed limitation "maintaining synchronization between the receiver circuit and the transmitter, without utilizing the host computer" is not supported in the specification. The word "computer" in the claims was intended to refer to host CPU 122 in Fig. 1. However, as pointed out by the Examiner, this wording is not consistent with the specification since host computer 106 includes receiver circuit 108, which is used for synchronization in the present invention. In order to correct this situation, claims 4, 13, 20 and 24 have been amended to clarify that synchronization is maintained without utilizing the microprocessor of the host computer. As stated at page 4, lines 1-2 of the specification, CPU 122 comprises the microprocessor of host computer 106. Although also rejected for the same reason, claim 16 was not so amended because it does not contain the limitation objected to (except to the extent that it contains such limitation by being dependent on claim 13). It is respectfully submitted that the claims, as amended, are fully supported by and consistent with the specification and therefore the rejection should be withdrawn.

Claim Rejection under 35 USC 102(b)

Claims 4, 7, 8, 13, 16, 17, 20, 21, 24 and 25 stand finally rejected as being anticipated by Maturi et al ("Maturi"). It is re-emphasized that Maturi teaches host microcontroller 18 (Fig. 3) directly involved in the synchronization of the system time clock and the values provided by PCR timestamps in the MPEG bitstream. For example, Maturi (e.g., col. 8, lines 6-30) teaches that pre-parser 22 (considered by the Examiner to be equivalent to Applicant's receiver circuit) generates a first interrupt to the host microcontroller 18 and, in response, host microcontroller 18 reads system time counter 38 to obtain an initial system clock time ("SCR0"). When the PCR is parsed from the transport layer, pre-parser 22 extracts this value ("SCR1"), which is compared to SCR0 to obtain the error between the actual and requested values of the system clock time. After decoding the PES header, microcontroller 18 reads the

value of the counter 38 (SCR2") and causes a new value to be set into counter 38 equal to SCR2+(SCR1-SCR0), thereby synchronizing counter 38 by compensating for the time required to decode the header.

Claims 4, 13, 20 and 24 have been amended to clarify that synchronization between the receiver circuit and the transmitter is maintained without utilizing the host microprocessor (CPU 122). In the present invention, synchronization is accomplished completely within the receiver circuit, e.g. using firmware in a transport controller. The present invention is particularly useful in applications where a direct memory access ("DMA") engine (element 119 in Fig. 1) is used to transfer elementary streams from the receiver circuit since with DMA data is transferred without requiring CPU intervention. Once the receiver circuit and transmitter are synchronized without using the host microprocessor, a system timestamp for an application system coupled with the decoder circuit (but not with the receiver circuit) is captured with the decoder circuit.

For the reasons described above, the amended claims clearly distinguish over Maturi and the amendment places the claims in condition for immediate allowance. Rejected claims 7, 8, 16, 17, 21 and 25, dependent on the amended claims, also contain this element and are similarly distinguished over Maturi. Accordingly, withdrawal of the rejection and allowance of the amended claims are respectfully requested.

Claim Rejection under 35 USC 103(a)

Claims 9, 18, 22, and 26 stand finally rejected as being obvious over Maturi. Claims 19 and 23 are rejected as being obvious over Maturi in further view of Dokic US 5699392. Each of these claims are dependent on one of the amended independent claims discussed above. Therefore, these claims incorporate the added limitation that the receiver circuit maintains synchronization between the receiver circuit and the transmitter without utilizing the host microprocessor. As previously discussed, neither Maturi and Dokic, alone or in combination, teaches or suggests this limitation. Accordingly, it is respectfully submitted that the amended claims avoid the rejection and are in condition for allowance.

CONCLUSION

It is respectfully submitted that entry of this amendment is proper under 37 CFR 1.116 (b) because all of the claims, if amended as proposed, avoid the rejections set forth in the final office action for the reasons set forth above, and therefore are in condition for allowance, or are placed in better condition for appeal. In addition, the only amendment that is proposed to the claims is to replace reference to "computer" with "microprocessor" (and to provide antecedent basis in the claim therefor). Accordingly, the proposed amendment does not raise new issues that would require further consideration and/or search. In light of the above, entry of this amendment and the issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 303-571-4000.

Respectfully submitted,

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